Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A peripheral management system, comprising a system chip, a peripheral I/O control device and a control management device, said control management device being electrically connected between said system chip and said peripheral I/O device in series, and asserting a first processing signal to said peripheral I/O control device in response to a control signal from said system chip in a normally operational state of said peripheral management system, and asserting a second processing signal to said peripheral I/O control device in response to an external control signal in a crash state of said peripheral management system.

2. (Original) The peripheral management system according to claim 1 wherein said peripheral management system is a part of a computer system.

3. (Original) The peripheral management system according to claim 1 wherein said control management device is a baseboard management controller (BMC).

4. (Original) The peripheral management system according to claim 1 wherein a bus applied to said peripheral management system is a low pin count (LPC) bus.

5. (Original) The peripheral management system according to claim 1 wherein said system chip is a south bridge chip.

6. (Original) The peripheral management system according to claim 1 wherein said peripheral I/O control device comprises a control management memory, a system BIOS and a super I/O control device.

7. (Original) The peripheral management system according to claim 6 wherein said control management memory is a flash memory, and said system BIOS is a flash memory.

8. (Original) The peripheral management system according to claim 6 wherein said super I/O control device is for controlling at least a keyboard, a mouse, a floppy disc drive and a communication port.

9. (Previously Cancelled)

10. (Previously Presented) The peripheral management system according to claim 1 wherein said external control signal is asserted by a remote terminal.

11. (Previously Cancelled)

12. (Previously Cancelled)

13. (Previously Cancelled)

14. (Previously Cancelled)

15. (Previously Presented) The peripheral management system according to claim 1 wherein said control management device asserts a third processing signal in a simulation control state.

16. (Original) The peripheral management system according to claim 15 wherein said third processing signal is transmitted from said control management device to said system chip in response to another external control signal.

17. (Original) The peripheral management system according to claim 16 wherein said peripheral I/O control device comprises a super I/O control device, and said another external control signal is a remote simulation control signal for simulating the input/output operation of said super I/O control device.

18. (Original) The peripheral management system according to claim 15 wherein said third processing signal is actively generated by said control management device to be exclusively provided for said system chip.

19. (Previously Cancelled)

20. (Previously Cancelled)

21. (Previously Cancelled)

22. (Previously Cancelled)

23. (Previously Presented) A peripheral management system, comprising a system chip, a system BIOS and a control management device, said control management device being electrically connected between said system chip and said system BIOS in series, and asserting a first processing signal to said system BIOS in response to a control signal from said system chip in a normally operational state of said system BIOS, and asserting a second processing signal to said system BIOS in response to an external control signal in an idle state of said system BIOS.

24. (Previously Presented) The peripheral management system according to claim 23 wherein said external control signal is a remote BIOS update request signal for updating said system BIOS so as to recover from said idle state to said normally operational state.

25. (Previously Presented) A peripheral management system, comprising a system chip, a super I/O control device and a control management device, said control management device being electrically connected between said system chip and said super I/O device in series, and asserting a first processing signal to said super I/O control device in response to a control signal from said system chip in a normally operational state of said system chip, and asserting a second processing signal to said super I/O control device in response to an external control signal in an idle state of said system chip.

26. (Previously Presented) The peripheral management system according to claim 25 wherein said external control signal is a remote super I/O control signal for controlling the input/output operation of said super I/O control device.